

Influence of active layer thickness, device architecture and degradation effects on the contact resistance in organic thin film transistors

C.A. Pons-Flores

*Departamento de Ingeniería Eléctrica, Centro de Investigación y de Estudios Avanzados del IPN
Gustavo A. Madero, Cd. de México, 07360, México.*

I. Mejía, M.A. Quevedo-López

*Department of Materials Science and Engineering, University of Texas at Dallas
Richardson, TX 75080, USA.*

C. Alvarado-Beltran

*Universidad Autónoma de Sinaloa
Los Mochis, Sinaloa, 81200, México.*

L.M. Reséndiz*

*Sección de Estudios de Posgrado e Investigación, UPIITA, Instituto Politécnico Nacional
Gustavo A. Madero, Cd. de México, 07340, México.*

(Received: July 6th, 2017; Accepted: September 12th, 2017)

We analyze the influence of three combined effects on the contact resistance in organic- based thin film transistors: a) the active layer thickness, b) device architecture and c) semiconductor degradation. Transfer characteristics and parasitic series resistance were analyzed in devices with three different active layer thicknesses (50, 100 and 150 nm) using top contact (TC) and bottom contact (BC) thin film transistor (TFT) configurations. In both configurations, the lowest contact resistance ($2.49 \times 10^6 \Omega$) and the highest field-effect mobility ($4.8 \times 10^{-2} \text{ cm}^2/\text{V}\cdot\text{s}$) was presented in devices with the thicker pentacene film. Top contact thin film transistors presented field-effect mobility values one order of magnitude higher ($4.8 \times 10^{-2} \text{ cm}^2/\text{V}\cdot\text{s}$) than bottom contact ones ($1 \times 10^{-3} \text{ cm}^2/\text{V}\cdot\text{s}$). Threshold voltage for top-contact thin film transistors was -3.1 V. After 2 months, performance in the devices degraded and presented an increase of one order of magnitude ($10^5 - 10^6 \Omega$) for BC-TFTs and two orders of magnitude ($10^6 - 10^8 \Omega$) for TC-TFTs in contact resistance.

Introduction

Organic thin film transistors (OTFTs) have attracted interest for large area electronic applications due to the compatibility with low cost and low temperature fabrication processes. Depending on the device configuration, several parasitic effects could limit its performance. Among the most important effects, parasitic series resistance has been reported to strongly affect the electrical performance of the thin film transistors (TFTs) [1]. In fact, as the resistance of the channel decreases, the contact resistance becomes increasingly important, in particular in short channel devices. Series resistance can be influenced by metal contact, film thickness, device architecture, substrate roughness, device processing, and temperature [2-6]. Therefore it is important to analyze the two typical contact configurations used for OTFTs: top-contact (TC) and bottom-contact (BC). For example, the deposition of the active layer in BC-TFTs is the last fabrication step; therefore the semiconductor is not exposed to other processes as in TC-TFTs. However, BC-TFTs have showed several drawbacks compared to TC-TFTs, as the application of a gate voltage induces a channel with a higher conductivity at the semiconductor/dielectric interface [7]. TC-TFTs have exhibited contact resistance (R_c) of about one order of magnitude higher than BC-TFTs [8] and R_c dependence on the pentacene/Au

thickness ratio [9].

Another important effect limiting the OTFT performance is the degradation of the active layer when exposed to ambient, as a result of oxygen diffusion in the bulk of the material. The oxygen absorption in the active layer degrades the current-voltage characteristics [10]. For pentacene OTFTs, researchers have found still functional devices with decreased performance in terms of field-effect mobility (μ), on-current, $I_{on/off}$ ratio and threshold voltage (V_T) shifting even after degradation [11-12].

Although researchers have analyzed the influence of the pentacene degradation in the performance of the OTFTs, they only focus in the main parameters such as μ and drain current (I_D) [13-14]. In this reports, it has been neglected other important parameters of equally importance; for example, the parasitic resistance. In general, different authors in different reports have described the characteristics of pentacene-based OTFTs in terms of active layer thickness [8,15,16], devices structure [1-2,7,16] and degradation [10-14]. However, a complete analysis for the same OTFT technology has not been reported.

In this study, the influences of three combined effects on the R_c : a) active layer thickness, b) device architecture and c) semiconductor degradation are investigated in pentacene-based OTFTs. This analysis can be applied to other organic dielectric/semiconductor systems. We fabricated TC and BC

* lresendiz@ipn.mx

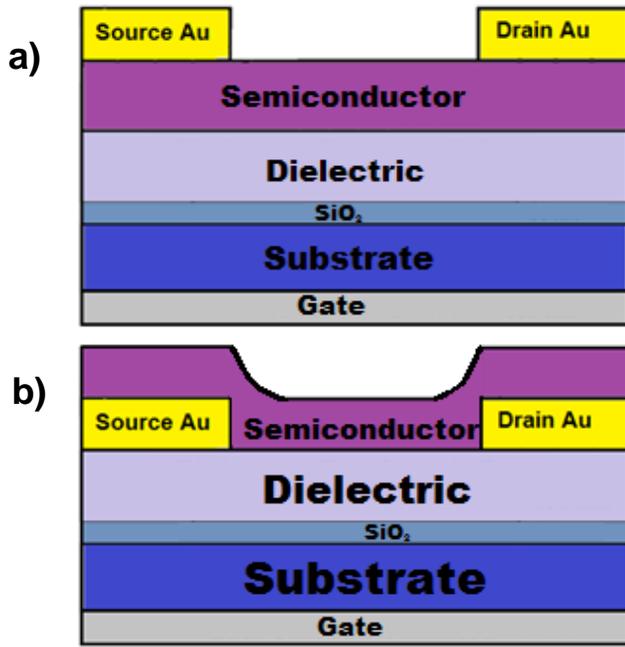


Figure 1. Cross-section of PTFTs with dielectric SiO₂/parylene bilayer. a) TC, b) BC.

TFT configurations with a SiO₂/parylene dielectric bilayer to minimize the leakage current. The stability and lifetime of the TFTs were analyzed.

Experimental details

OTFTs were fabricated using a highly doped p-type silicon wafer with a back common aluminum layer used as gate electrode. First, 190 nm of parylene-C were deposited by chemical vapor deposition on top of 50 nm of thermally grown SiO₂ to form a gate dielectric bilayer. SiO₂ helps to reduce the gate leakage current, whereas parylene-C improves the dielectric/semiconductor interface with pentacene [17,18]. Next, aluminum gate metal was deposited on the backside of the wafer. Then, three pentacene film thicknesses 50 nm, 100 nm and 150 nm were sublimated while the substrate was kept at room temperature. In order to define BC and TC configuration the 150 nm thickness contacts were deposited, using a shadow mask, by e-beam evaporation prior to, or after, the pentacene deposition, respectively. BC-TFTs and TC-TFTs are shown in Figure 1a) and 1b), respectively.

OTFTs were electrically characterized immediately after fabrication using a Keithley 4200 semiconductor characterization system. OTFTs were also measured one and two months after being stored at room temperature in dark ambient conditions.

Results and discussion

Figure 2 shows the transfer characteristics of BC-TFTs and TC-TFTs fabricated with three different pentacene thicknesses. As can be seen, I_D is higher for BC-TFTs (open symbols) and the devices remained always on, which is the

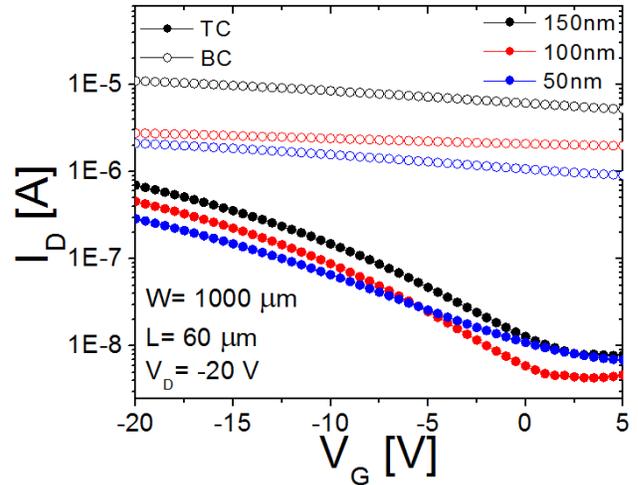


Figure 2. BC vs. TC Pentacene TFTs transfer characteristic.

result of a less resistive path for the current between source and drain compared to TC-TFTs (solid symbols) configuration. In BC-TFTs, the holes are injected/collected directly from the sidewall of the electrodes to the channel. Therefore, the current flows parallel to the polymer chains and the overall resistance the carriers experience in BC-TFTs is lower than in TC-TFTs, where the carriers need to flow vertically from the contact through the pentacene bulk in order to reach the channel, resulting in an additional resistance component that limits the electrical current.

V_T and μ for TFTs were calculated from the extrapolation and slope of the $\sqrt{I_D}$ vs. V_G curve measured in saturation respectively, following the expression for I_D in MOS transistors:

$$I_D = C_{ox} \cdot \mu \cdot \frac{W}{L} \cdot \frac{(V_G - V_T)^2}{2} \quad (1)$$

where C_{ox} is the dielectric capacitance per unit area; W is the channel width and L is the channel length.

Calculated V_T for BC-TFTs is more positive compared to TC-TFTs, due to the higher channel and bulk conductivity resulting from the higher carrier injection and the direct contact between the accumulation layer and the source-drain (S-D) contacts that does not allow to completely close the channel [19]. Carrier injection from S-D electrodes in BC-TFTs is expected to be higher; however, with a smaller effective contact area compared to TC-TFTs. This V_T increment in BC-TFTs is due to overestimations for short channel devices using the square-root-of-current-extrapolation (SRE) method [20], which is greatly affected by series resistances [21].

TC-TFTs presented mobilities one order of magnitude higher ($4.8 \times 10^{-2} \text{ cm}^2/\text{V}\cdot\text{s}$) than BC-TFTs ($1 \times 10^{-3} \text{ cm}^2/\text{V}\cdot\text{s}$). Changes in mobility on BC-TFTs have been attributed to contact (semiconductor/metal) effects due to a dipole barrier that can shift the vacuum level upward by more than 1 eV, avoiding carriers to reach the HOMO level [22-24]. However, mobility is not dependent on the contacts used in the TFT and is normally dictated by the dielectric/semiconductor interface in both TC and BC structures. Therefore, the differences in the calculated values

Table 1. Behavior of μ for devices with $L = 80 \mu\text{m}$.

Thickness (nm)	μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	
	TC	BC
50	8.7×10^{-3}	4.41×10^{-3}
100	1.4×10^{-2}	5.41×10^{-3}
150	4.8×10^{-2}	8.59×10^{-3}

for mobilities between the two structures could be misleading and the result of the use of a TFT model that does not include a term related to the contact effects and bulk current. Also, we observed for all the pentacene thicknesses a channel length dependence in BC-TFTs, as μ increased almost an order of magnitude for larger channel lengths, whereas for TC-TFTs μ remained almost constant for all the channel lengths. Since the contact effects are not considered in the model, it can be assumed that more accurate values are obtained for larger channels ($80 \mu\text{m}$) where the contact resistance effects are less important (Table 1).

Contact Resistance

R_c was obtained from experimental data at $V_D = -3.5 \text{ V}$ in the linear regime using the transmission line method (R vs. L) [25]. TC-TFTs presented a higher contact resistance ($10^7 \Omega$) than BC-TFTs ($10^5 \Omega$). R_c seems to be reduced as V_G is increased for TC-TFTs, whereas for BC-TFTs, R_c remained in the same order of magnitude for all the pentacene thicknesses, see Figure 3. Higher contact resistance in TC-TFTs could be due to an additional resistance presented in the structure from the vertical transport through the bulk of pentacene that limits carrier injection from the semiconductor/contact interface to the channel.

When V_G becomes higher, the barrier the carriers see is reduced and the conduction is no longer limited by the bulk, reducing R_c . In BC-TFTs this barrier is very small and there is no V_G dependence [25]. Nevertheless, both configurations presented the same trend of contact resistance in terms of semiconductor thickness, where the thinnest TFTs presented the highest contact resistance. This effect can be related to

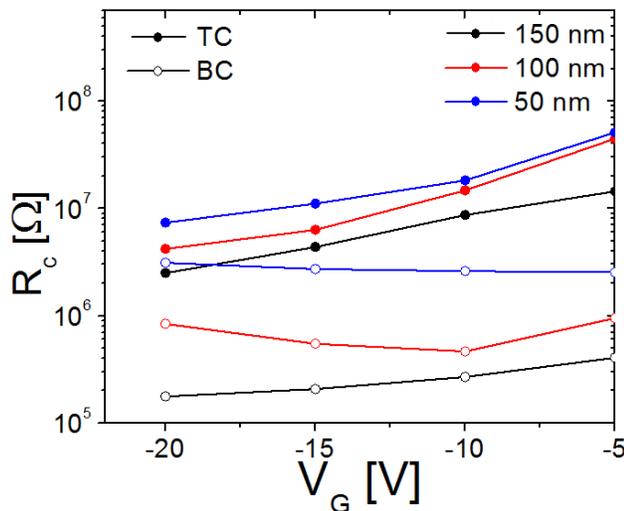


Figure 3. Contact resistance in top and bottom contact devices.

thickness ratio between the S-D contacts and the semiconductor. Thinner semiconductor films do not cover entirely the height of the contacts in case of the BC-TFTs, therefore the contacted area is smaller compared to thicker semiconductor films. In case of the TC-TFTs, the increase of the contact resistance with decrease in film thickness may be due roughness and grain size of the polycrystalline semiconductor. Results reported in [26] indicate that grain size increases with increasing thickness of polycrystalline films. In [27,28] was shown an increase in the mobility with increasing grain size and decreasing surface roughness. And, a decrease of the contact resistance was observed in [29] due to an increase in field-effect mobility of pentacene TFTs.

Degradation

Figure 4 shows the transfer curves for TC-TFTs with 150 nm pentacene films (devices with higher mobility) after one and two months of being fabricated. Degradation produced a decrease in μ and a shift in the V_T . Mobility decreased almost an order of magnitude per month in both configurations. V_T on TC-TFTs tends to increase and the maximum on-current is reduced by an order of magnitude per month, as shown in Table 2, nevertheless $I_{on/off}$ ratio remains in the same order of magnitude after 2 months. Similar results have been reported in [30,31], where a drop in field-effect mobility, threshold voltage and drain current was obtained as a result of active layer degradation after 1320 h the pentacene TFTs were fabricated.

Figure 5 shows contact resistance for both configurations. In both cases, contact resistance becomes higher after two months, which indicates also degradation at the semiconductor/metal interface that follows the same trend in terms of V_G for each TFT configuration.

This behavior might be due to OH and C-H₂ defects in pentacene after the material has been exposed to oxygen and humid environments. These defects modify the structure of the pentacene molecule and produce localized states in the bandgap as well as hole trapping at the grain boundaries, where C-H₂ defects form a C₂₂H₁₅ molecule and one of the C atoms becomes fourfold coordinated. On the other hand, OH

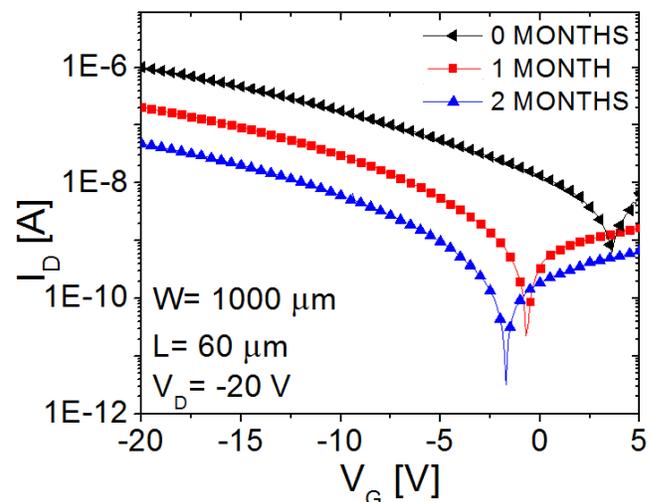


Figure 4. Transfer curves in saturation after 0, 1 and 2 months.

Table 2. Behavior of μ , I_D , $I_{on/off}$ ratio and V_T considering two months analysis.

Month	μ (cm ² /V·s)		V_T (V)		I_{Dmax} (A)		$I_{on/off}$ ratio (A)	
	TC	BC	TC	BC	TC	BC	TC	BC
0	3×10^{-2}	1.7×10^{-2}	-3.1	64.56	1.01×10^{-6}	2.26×10^{-6}	9.83×10^1	12.7×10^{-1}
1	8×10^{-3}	3×10^{-3}	-3.3	27.04	2.04×10^{-7}	7.8×10^{-7}	8.23×10^1	17.9×10^{-1}
2	2×10^{-3}	4×10^{-4}	-4.96	16.87	4.79×10^{-8}	1.1×10^{-6}	6.29×10^1	15.9×10^{-1}

forms a C₂₂H₁₃O molecule in which there is a C-O double bond by replacing one of the hydrogen atoms by an oxygen atom [32].

Considering also that the morphology of polycrystalline pentacene films is relatively open, with large crevices between the grains that run almost all the way down to the first few monolayers on the substrate [33] and that pentacene is highly hydrophobic, H₂O molecules can easily diffuse into crevices modifying the morphology of the film, inducing a phase transition from a thin film phase to a bulk-like phase [34]. Also, interacting with the trapped carriers at the grain boundaries by limiting the charge transport and therefore, affecting the performance of the devices [35].

R_c increases with time and conductivity through the channel is reduced by the limited carrier transport. Oxygen

located in the bulk of the film can continue absorbing oxygen from ambient, as it has been found this for the same semiconductor/contact thickness and for thinner pentacene films. In the thickest TC-TFTs, R_c increases more over time because it is more likely to have more defects and traps with increasing grain size. In the case of the BC-TFTs with 100 nm pentacene films R_c increases more rapidly maybe due to humidity does not reach the dielectric/semiconductor interface and pentacene films continue absorbing oxygen from the ambient, also defects may be lower, not affecting as much as the TC-TFTs performance.

Conclusions

In summary, an analysis due to the effects of the active layer thickness, device architecture and pentacene degradation on the R_c of the OTFTs was presented. Devices presented thickness dependence; this may be due roughness and grain size of the active layer. Devices with thicker active layer presented a better performance, TC-TFTs presented higher mobility as high as 4.8×10^{-2} cm²/V·s compared to BC-TFTs (4.41×10^{-3} cm²/V·s). Also, the results were less sensitive to geometry of the device (channel length). In terms of configuration, TC-TFTs show a more resistive channel ($10^7 \Omega$) and a V_G dependence compared to BC-TFTs for almost an order of magnitude ($10^5 \Omega$). This effect might be due to BC-TFTs have a smaller Au-contact area and therefore a smaller carrier injection at the contact/semiconductor interface. We have to consider that BC-TFTs have a metal-insulator-metal structure, where S-D contacts are directly in contact to the channel and dielectric layer is exposed to contact deposition process, whereas TC-TFTs have a metal-insulator-semiconductor structure where the active layer is exposed to the contact deposition process. Despite oxygen and moisture from the environment contributes to the active layer degradation, which affects to the performance of the device, OTFTs still be functional after 2 months, nevertheless with a decrease of an order of magnitude in terms of μ (10^{-2} - 10^{-3} cm²/V·s) and I_{Dmax} (1×10^{-6} - 4.79×10^{-8} A), while R_c increase two orders of magnitude (2.49×10^6 - $1.1 \times 10^8 \Omega$) for TC-TFTs and an order of magnitude (1.76×10^5 - $1.57 \times 10^6 \Omega$) for BC-TFTs, due to hole trapping and oxygen absorption in the active layer.

Acknowledgements

This work was supported by SIP-IPN project 20171781 and partially funded by CONACYT project CB-2014/240103.

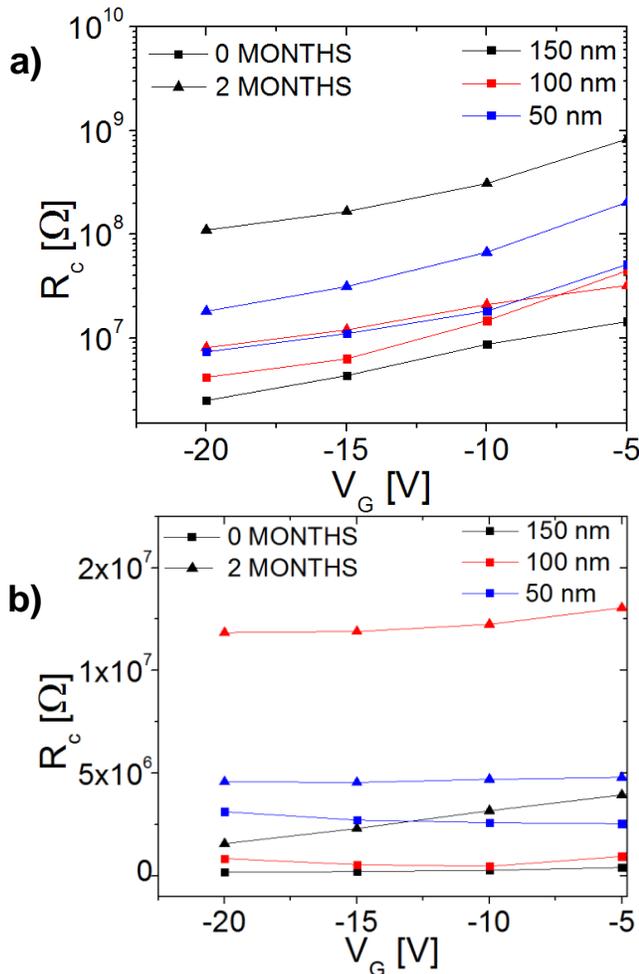


Figure 5. Contact resistance in a) TC and b) BC, after 0 and 2 months with different thicknesses.

References

- [1]. D. Gupta, M. Katiyar, D. Gupta, *Org. Electron.* **10**, 775 (2009).
- [2]. D.J. Gundlach, L. Zhou, J.A. Nichols, T.N. Jackson, P.V. Necliudov, M.S. Shur, *J. Appl. Phys.* **100**, 024509 (2006).
- [3]. S. Lee, S.J. Kang, G. Jo, M. Choe, W. Park, J. Yoon, T. Kwon, Y.H. Kahng, D.Y. Kim, B.H. Lee, T. Lee, *Appl. Phys. Lett.* **99**, 083306 (2011).
- [4]. H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C.D. Sheraw, J.A. Nichols, T.N. Jackson, *Solid-State Electron.* **47**, 297 (2003).
- [5]. J. Park, J.M. Kang, D.W. Kim, J.S. Choi, *Thin Solid Films* **518**, 6232 (2010).
- [6]. Y.J. Lin and B.C. Huang, *Microelectron. Eng.* **103**, 76 (2013).
- [7]. F. Li, A. Nathan, Y. Wu and B. S. Ong, *Organic Thin Film Transistor Integration: A Hybrid Approach (Wiley, Weinheim Germany, 2011)*.
- [8]. G.B. Blanchet, C.R. Fincher, M. Lefenfeld, *Appl. Phys. Lett.* **84**, 296 (2004).
- [9]. S. Gowrisanker, Y. Ai, M.A. Quevedo-Lopez, H. Jia, H.N. Alshareef, E. Vogel, B. Gnade, *Appl. Phys. Lett.* **92**, 153305 (2008).
- [10]. V.H. Martinez-Landeros, G. Gutierrez-Heredia, F.S. Aguirre-Tostado, M. Sotelo-Lerma, B.E. Gnade, M.A. Quevedo-Lopez, *Thin Solid Films* **531**, 398 (2013).
- [11]. Ch. Pannemann, T. Diekmann, U. Hilleringmann, *J. Mat. Res.* **19**, 1999 (2004).
- [12]. D. Simeone, M. Rapisarda, G. Fortunato, A. Valletta, L. Mariucci, *Org. Electron.* **12**, 447 (2011).
- [13]. C.R. Kagan, A. Afzali, T. O. Graham, *Appl. Phys. Lett.* **86**, 193505 (2005).
- [14]. Y. Hu, G. Dong, Y. Liang, L. Wang, Y. Qiu, *Jpn. J. Appl. Phys.* **44**, L938 (2005).
- [15]. L. Mariucci, D. Simeone, S. Cipolloni, L. Maiolo, A. Pecora, G. Fortunato, S. Brotherton, *Solid-State Electron.* **52**, 412 (2008).
- [16]. B. Kumar, B.K. Kumar, Y.S. Negi, *IET Circuits Devices Syst.*, **8**, 131 (2014).
- [17]. K.N.N. Unni, S. Dabo-Seignon, J.M. Nunzi, *J. Mater. Sci.* **41**, 1865 (2006).
- [18]. K. Tsukagoshi, I. Yagi, K. Shigeto, K. Yanagisawa, J. Tanabe, Y. Aoyagi, *Appl. Phys. Lett.* **87**, 183502 (2005).
- [19]. Y.W. Wang, D.Z. Liu, M.Y. Hong, H.L. Cheng, *Proc. of SPIE* **7417**, 74171F (2009).
- [20]. M. Tsuno, M. Suga, M. Tanaka, K. Shibahara, M. Miura-Mattausch, M. Hirose, *IEEE Trans. Electron. Devices* **46**, 1429 (1999).
- [21]. D. Boudinet, G.L. Blevennec, C. Serbutoviez, J.M. Verilhac, H. Yan, G. Horowitz, *J. Appl. Phys.* **105**, 084510 (2009).
- [22]. W.T. Wondmagegn, N.T. Satyala, R.J. Pieper, M.A. Quevedo-Lopez, S. Gowrisanker, H.N. Alshareef, H.J. Stiegler, B.E. Gnade, *J. Comput. Electron.* **10**, 144 (2011).
- [23]. N. Koch, A. Kahn, J. Ghijsen, J.J. Pireaux, J. Schwartz, R.L. Johnson, A. Elschner, *Appl. Phys. Lett.* **82**, 70 (2003).
- [24]. R.T. Tung, *Phys. Rev. B*, **64**, 205310 (2001).
- [25]. P.V. Necliudov, M.S. Shur, D.J. Gundlach, T.N. Jackson, *Solid-State Electron.* **47**, 259 (2003).
- [26]. H.L. Cheng, Y.S. Mai, W.Y. Chou, L.R. Chang, X.W. Liang, *Adv. Funct. Mater.* **17**, 3639 (2007).
- [27]. R. Matsubara, N. Ohashi, M. Sakai, K. Kudo, M. Nkamura, *Appl. Phys. Lett.* **92**, 242108 (2008).
- [28]. B. Bräuer, R. Kukreja, A. Virkar, H.B. Akkerman, A. Fognini, T. Tylliszczac, Z. Bao, *Organic Electron.* **12**, 1936 (2011).
- [29]. E.J. Meijer, G.H. Gelinck, E. van Veenendaal, B.H. Huisman, D.M. de Leeuw, T.M. Klapwijk, *Appl. Phys. Lett.* **82**, 4576 (2003).
- [30]. T. Ahn, H.J. Suk, J. Won, M.H. Yi, *Microelectron. Eng.* **86**, 41 (2009).
- [31]. J. Li, H.P. Lin, F. Zhou, W.Q. Zhu, X.Y. Jiang, Z.L. Zhang, *Curr. Appl. Phys.* **12**, 280 (2012).
- [32]. J.E. Northrup, M.L. Chabiny, *Phys. Rev. B* **68**, 041202(R) (2003).
- [33]. C.D. Dimitrakopoulos, D.J. Mascaró, *IBM J. Res. Dev.* **45**, 11 (2001).
- [34]. D.J. Gundlach, T.N. Jackson, D.G. Schlom, S.F. Nelson, *Appl. Phys. Lett.* **74**, 3302 (1999).
- [35]. Z.T. Zhu, J.T. Mason, R. Dieckmann, G.G. Malliaras, *Appl. Phys. Lett.* **81**, 24 (2002).