

Memristance effect of metal-insulator-metal structures using Al_2O_3 film as active layer for emergent memory devices

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(Recibido: 2 de septiembre de 2013; Aceptado: 29 de diciembre de 2014)

The *memristor effect* (cyclic switching from a High-Resistance State to a Low-Resistance State and viceversa) and a conductivity/resistivity window ($I_{\text{OFF}}/I_{\text{ON}}$ ratio) of more than 4 orders of magnitude have been obtained in Metal-Insulator-Metal (MIM) structures that use Al_2O_3 as oxide layer after cyclic I-V measurements. Before initial breakdown, different carrier conduction properties are found when using whether a highly reactive or a highly inert metal as the bottom electrode of the memory structure. These carrier conduction properties for the MIM structure are also affected by changing the deposition conditions of the bottom electrode (by changing the average roughness of its surface) or by using different Al_2O_3 thickness. Most importantly, because of the low thermal budget used for fabrication of these devices (only 300°C), they have the potential to be vertically integrated as memory cells in higher metallization levels of a CMOS-based Back-End-Of-Line (BEOL) processing. This is important since it would promote real 3-D integration of memory devices for advanced circuit manufacturing.

Keywords: Memristance Effect; MIM structures; Atomic-Layer Deposition; Al_2O_3 ; BEOL Processing; Conduction Mechanisms, RRAM Devices

1 Introduction

Resistive-switching Random Access Memory (RRAM) devices have attracted considerable attention in recent years for their superior characteristics, including their simple memory structure which is usually composed of Metal-Insulator-Metal (MIM) stacks, deep scalability, ultra-low power consumption, fast write/erase speed, and long retention times [1-4]. For RRAM devices, metal oxides based on high dielectric constant materials (*high-k*) are widely used because of their resistive switching properties and their general physical characteristics which make them compatible with a silicon CMOS-BEOL fabrication process [2-4]. However, several improvements are still needed before RRAM devices become attractive to the semiconductor industry: higher endurance cycles, adequate write/erase margins, multi-level resistance storage and most importantly, understanding and correlating the precise mechanisms required for resistive switching or their fabrication process conditions.

A better understanding of the physics related to resistive switching will be helpful in achieving these goals. Even though it is widely recognized that resistive switching mainly originates from the forming/rupture of ultra-thin conductive filaments in the oxide film, the precise physics and chemistry of this switching behavior is ambiguous and remains fully unanswered. Ideally, RRAM switching modes can be classified in two groups: *unipolar switching*, which means the resistive switching depends on the amplitude of the applied voltage but not on the polarity; and *bipolar switching*, which means the resistive switching relies on the polarity of the applied voltage bias [5]. During switching, the memory resistance states can be changed

from a High Resistance State (HRS) to a Low Resistance State (LRS) by SET and RESET voltage pulses respectively.

In an effort to better understand the RRAM's switching phenomena, we present the electrical characteristics of MIM structures varying some parameters in their fabrication process as well as using different materials as bottom electrode; all to assess the conduction mechanisms of carriers just before the initial switching occurs.

2 Experimental Procedures

For all samples, glass slides were used as substrates which were cleaned by sequential ultrasonic cleanings in acetone, methanol, and iso-propanol; then all the substrates were rinsed with deionized water and dried with pure nitrogen flow. Two different MIM structures were obtained: $\text{Al}/\text{Al}_2\text{O}_3/\text{Al}$ and $\text{Al}/\text{Al}_2\text{O}_3/\text{W}$ stacks. First, aluminum (400 nm in thickness) was used as bottom electrode in an initial set of samples. Tungsten (500 nm in thickness) was used as bottom electrode in another set. Both metals for the bottom electrode were deposited by E-beam evaporation under ultra-high vacuum conditions. Then, Al_2O_3 was deposited directly on the bottom electrode by Atomic-Layer Deposition (ALD, Savannah-S100 system from Cambridge-Nanotech) using H_2O and Trimethyl-Aluminum (TMA) as precursor gases. At a growth temperature of 250°C , an average Al_2O_3 thickness of 10nm and 20nm were obtained. Finally, aluminum was used as top electrode for all structures (500 nm in thickness) and it was deposited by E-beam evaporation directly on Al_2O_3 . After MIM fabrication and lithography process (for gate pattern definition), a thermal treatment in

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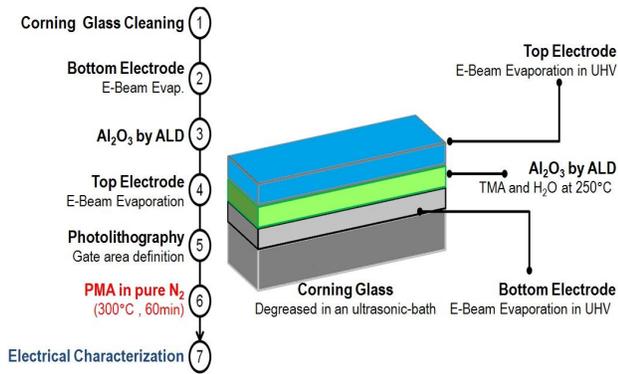


Figure 1. Process flow and schematic of the final MIM structure fabricated at low thermal budget on glass.

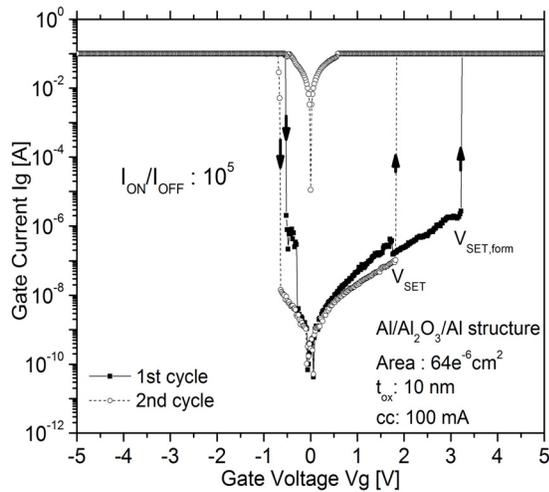


Figure 2. Bipolar resistive switching of MIM structures (Al/Al₂O₃/Al) fabricated at 300°C on glass. The I_{ON}/I_{OFF} ratio for this structure is slightly higher than 10^6 .

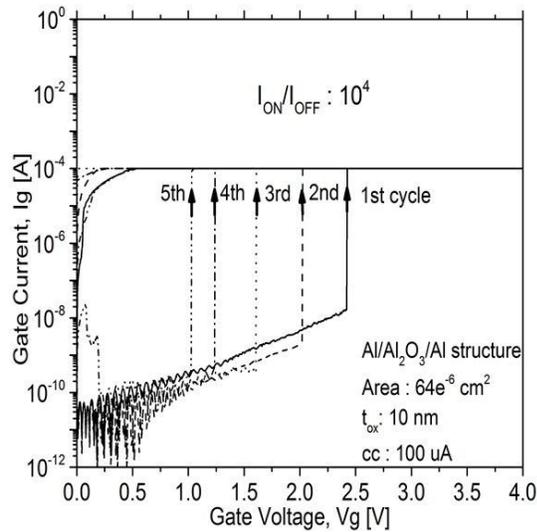


Figure 3. Unipolar resistive switching in MIM structures (Al/Al₂O₃/Al). The current compliance (CC) plays a crucial role for controlled switching behavior.

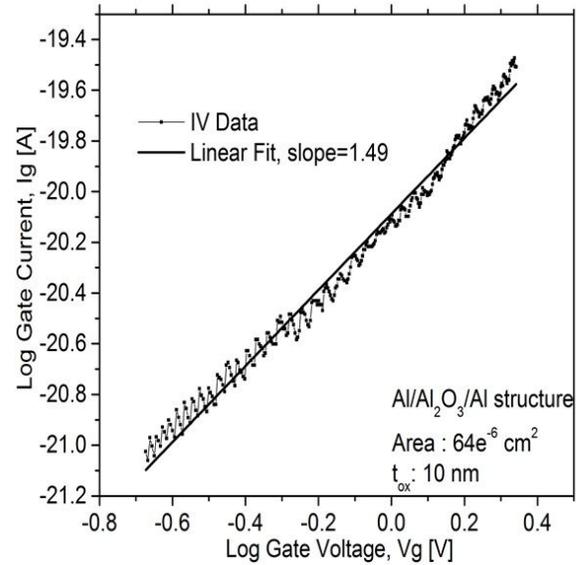


Figure 4. The linear fitting for the I-V characteristics of Al/Al₂O₃/Al suggest a TFL conduction mechanism.

N₂ (99.999% purity) at 300°C was applied to all samples and this was the maximum processing temperature used during fabrication of these structures. The area for all devices is 64e⁻⁶ cm².

All samples were electrically characterized using a Keithley Model 82-DOS Simultaneous C-V system in order to obtain the dielectric constant and capacitance-voltage characteristics (frequency range between 1kHz to 3MHz). A Semiconductor Device Analyzer (SDA, B1500A from Agilent) was also used in order to measure the current-voltage characteristics and obtain the breakdown electric field as well as the carrier conduction mechanisms before initial breakdown (before switching to the initial LRS condition). The process flow and the schematic of the final structure are both shown in figure 1.

3 Results and Discussion

The switching effect in MIM structures begins with a voltage or current-controlled forming process (V_{FORM} , I_{FORM}) that changes a fresh device from an initial HRS to a LRS condition and which is usually created by a hard breakdown event during electroforming of an ultra-thin and conductive filament (CF) that connects both electrodes of the MIM device [5-8]. Usually, a voltage sweep is applied to the top electrode (with the bottom electrode grounded) in order to create/dissolve this conductive filament (CF) inside the metal oxide film. Figure 2, shows that the FORMING voltage (V_{FORM}) of the memory cell is slightly larger than the SET voltage (V_{SET}) and the initial current in the HRS is smaller compared to the current in the LRS as expected. Each electrical test for the same MIM device (in this case, an Al/Al₂O₃/Al device) consists of applying a double sweep of voltage. First, we sweep the applied voltage from -5 V to +5 V, with a maximum compliance current of 100mA (fixed directly by the SDA). Here, it is important to notice that limiting the maximum current

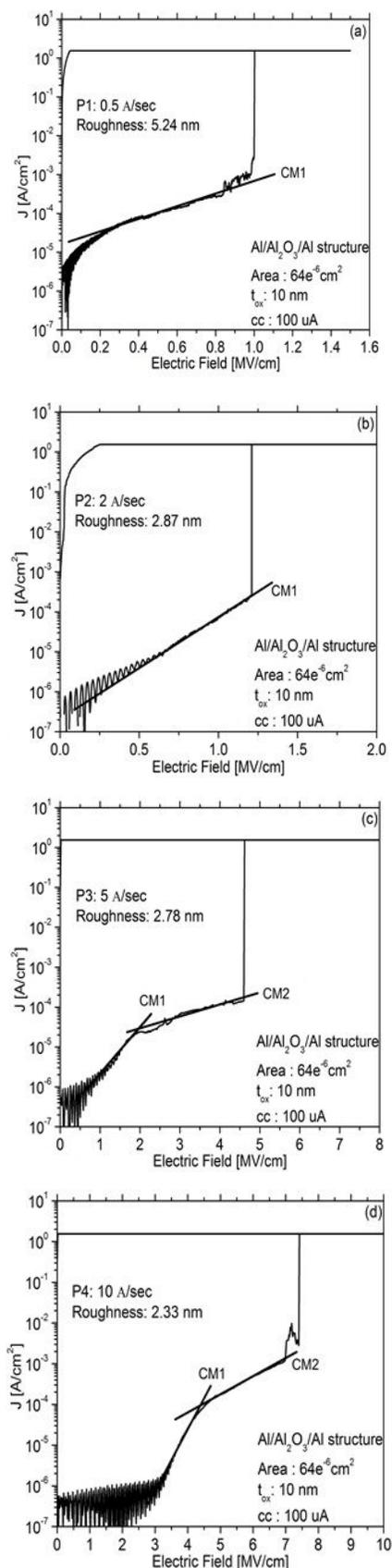


Figure 5. Different conduction mechanisms in MIM structures (Al/Al₂O₃/Al) with deposition different ratio for the initial aluminum layer (bottom electrode).

flowing through the device, helps to prevent a permanent damage on its oxide. For these initial I-V characteristics, the obtained behavior is similar to that of bipolar switching. The first sweep shows that the memory device is initially in the LRS (ON, reaching the current limit) and when the voltage is reduced in magnitude, the device then switches to the HRS (OFF), all during the negative polarity of applied voltage. For the positive polarity, the device shows an opposite conduction behavior. Now, when the voltage sweeps back to -5 V (to complete one full sweep cycle), the device is kept in the LRS. For a new full sweep cycle, the whole behavior is also observed although the V_{SET} is now reduced. Some authors suggest that in bipolar switching, the LRS is due by Joule heating and thermal diffusion of ions and defects [9-13].

Figure 3 shows that the degradation in the MIM's switching characteristics (from HRS to LRS) when using an increasing number of sequential I-V cycles is mainly observed as a reduction in V_{SET} . This limit in the endurance of these memory devices (lower V_{SET}) can be related to the generation of additional or even, a broader CF. Because the gate area of this device is considerably large, cyclic switching related to more than one CF will introduce excessive variability in the SET and RESET voltages and it must be considered an early failure mode [7] since some CF could not dissolve [13-14]. Additional generation and/or incomplete dissolution of CF's are thought to be related to the amount of current flowing through the device and which could be easily limited by adjusting the compliance current limit (CC) within the SDA. In figure 3, we also observe unipolar behavior, which is obtained by applying sequential voltage sweeps through the MIM device. Therefore, these memory devices can have two types of switching modes: unipolar and bipolar. Each switching mode will depend mainly on the bias conditions and also, the magnitude of compliance current that will limit the total current after breakdown [15].

Is important to emphasize that reliable RRAM memory device must ensure endurance cycles beyond two orders in magnitude. Our devices with Al/Al₂O₃/Al structure (figures 2 and 3) have a conductivity window (I_{ON}/I_{OFF}) greater than 10^4 in magnitude for both modes of operation. This broader relationship between the OFF state (HRS) and ON state (LRS) is very important because it increases the reliability to maintain the stored logic states within this memory device for a long time.

The degradation of memristive effect in our devices is a limiting factor, however the purpose of this work is to show that using a simple MIM structure and especially low thermal budget used for fabrication, it's possible in the future integration of these devices in BEOL stage for the fabrication of an IC.

On the other hand, we suggest that unipolar behavior in our devices is due to some specific conduction mechanisms before the breakdown events occur. To further analyze the conduction mechanism of these memory devices, their IV characteristics before breakdown were fitted to different conduction models: Fowler-Nordheim tunneling (F-N), trap-assisted tunneling (TAT), space-charge-limited-current

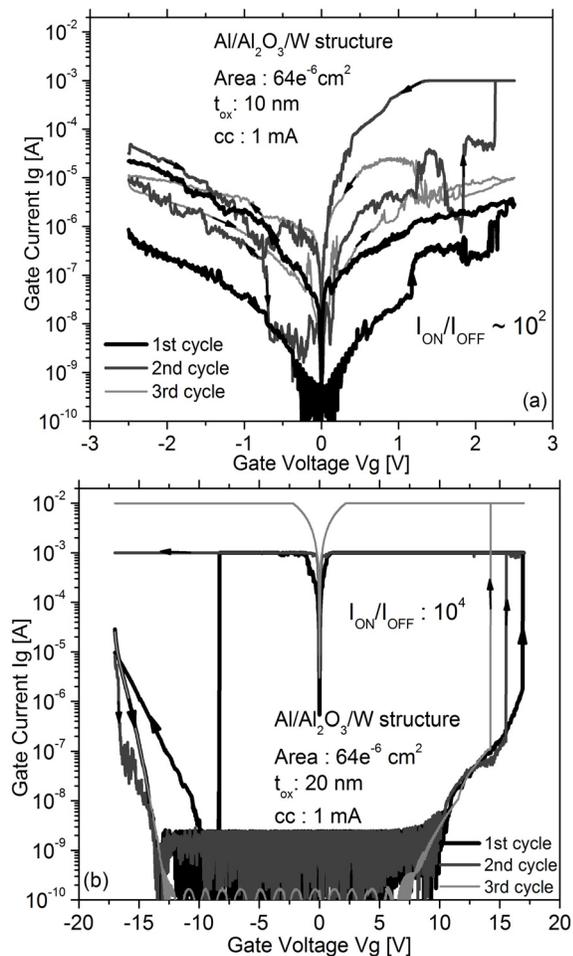


Figure 6. Resistive switching in MIM structures using an inert counter electrode.

(SCLS), Poole-Frenkel (P-F) and thermionic-emission model (TE). The best linear fitting is shown in Fig. 4, which indicates that the conduction before breakdown is composed by two limiting mechanisms: ohmic and TFL (trap-filled-limit).

Conduction by TFL mechanism [16-18] may be responsible for generating unipolar behavior in our devices.

Here, the traps inside the oxide have a major role in the transport of carriers since they would allow generation of additional conductive filaments which in turn, can be dissolved by lowering the electric field.

As surely inferred, the Metal/ Al_2O_3 interface is also of great importance for proper electronic conduction of carriers. Figure 5 shows different conduction processes for similar MIM structures ($\text{Al}/\text{Al}_2\text{O}_3/\text{Al}$). Here, the deposition ratio for the last portion of the first aluminum layer (bottom electrode) changed as follows:

P1: 0.5 Å/sec for aluminum, figure 5(a).

P1: 2 Å/sec for aluminum, figure 5(b).

P1: 5 Å/sec for aluminum, figure 5(c).

P1: 10 Å/sec for aluminum, figure 5(d).

These devices present unipolar switching mode. Here, we only show the first sweep cycle for comparison of the conduction mechanisms in our samples in a clearer, simpler

way. In figure 5(a), the structure presents a single conduction mechanism where the best linear fitting was found to be governed by the ohmic model [15-18]. In figure 5(b), the MIM structure presents a single conduction mechanism too. Here, the TFL model is the best fit, while the breakdown electric field is slightly greater compared to that of process 1. In figure 5(c), we notice that the MIM structure presents two conduction mechanisms: CM1 and CM2, corresponding to ohmic conduction and TFL respectively. Finally, in figure 5(d) we notice that two different conduction mechanisms appear as well while the best fitting gave the following carrier conduction mechanisms: TFL (CM1) and Poole-Frenkel (CM2).

By using different e-beam evaporation conditions that would increase the deposition ratio of the final portion of this aluminum layer (bottom electrode), we promote obtaining aluminum surfaces having different morphological and structural characteristics. This way, different conduction mechanisms during resistive switching are observed. It is highly suggestive to correlate the difference in conduction processes to the surface and therefore, interfacial roughness present in every Metal/ Al_2O_3 interface. Nevertheless, it is also important to consider the chemical changes occurring at these interfaces since lower or higher interfacial roughness would promote different chemical reactions creating interfacial layers (IL) of different characteristics.

On the other hand, some memory devices consist of an active electrode (AE) which acts as a source of mobile cations and an electrochemically inert counter-electrode (CE, usually Pt or W) where the cations get reduced to build up the metallic filament [2,15,19-20]. The mechanism for memristance effect in this type of memory device is widely accepted as a redox reaction which involves the oxidation of the AE atoms to produce mobile cations that migrate inside the thin oxide film and are reduced at the CE to form a metallic filament inside the thin oxide film (ON state), and finally, the dissolution and/or rupture of this metallic filament (OFF state) [2, 20-22]. Fig. 6 shows the I-V characteristics for the remaining $\text{Al}/\text{Al}_2\text{O}_3/\text{W}$ structures. Al_2O_3 has thickness of 10nm for Fig. 6(a) and 20 nm for Fig. 6(b).

In figure 6(b), we notice large electrical instabilities and variations in V_{SET} , V_{RESET} for many of the measured samples. These variations in V_{SET} , V_{RESET} are mainly due to large roughness variations of the Metal/ Al_2O_3 interfaces and which could be related to formation of stacking faults during evaporation of these metals at ultra-high vacuum conditions [7,12,15]. By doubling the Al_2O_3 thickness, the variations in V_{SET} , V_{RESET} are reduced notably because a thicker oxide would screen-out the surface roughness of both the bottom and top electrodes. In this case the voltage needed to create cyclic resistive switching between HRS and LRS is greater than 13 V, which means that its implementation into a CMOS BEOL process is quite limited. Therefore, it is necessary to minimize the surface roughness of the inert electrode so that smaller oxide thickness can be used and therefore, lower operating voltages.

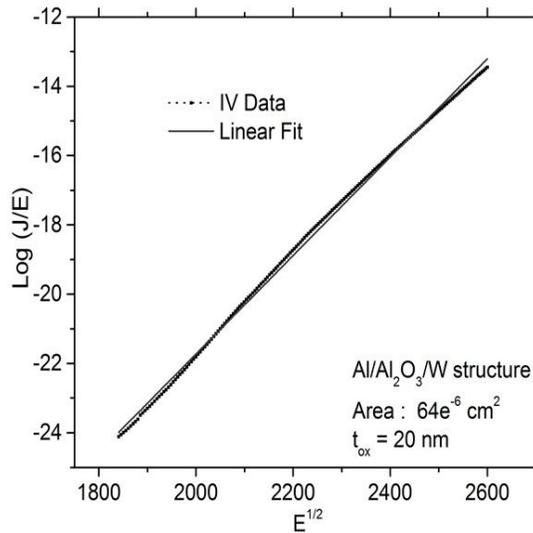


Figure 7. The linear fitting for the I-V characteristics of Al/Al₂O₃/W suggest Poole-Frenkel conduction.

A linear fitting of the I-V curve for the Al/Al₂O₃/W structure (Al₂O₃= 20 nm, before breakdown) is shown in Figure 7. Here the dominant conduction mechanism is Poole-Frenkel. In a similar way to the Al/Al₂O₃/Al structure, traps inside the oxide have a major role in the transport of carriers. After filling-up these traps, they would allow generation of additional conductive filaments.

It is important to mention that both devices (Al/Al₂O₃/Al and Al/Al₂O₃/W) show that there is no switching between HRS and LRS until both SET and RESET voltages are reached. This ensures that the stored information will not be lost even if parasite voltages (lower than V_{SET} and V_{RESET}) are developed or applied on the integrated circuit. Fig. 8 shows the dependence of gate capacitance density C_g on frequency after C-V measurements at room temperature for MIM structures having 10nm and 20nm in Al₂O₃ thickness respectively. It is clearly shown that for higher frequencies (up to 3 MHz), lower capacitance density C_g are obtained. Also, the dielectric constant relative to Al₂O₃ extracted from the C-V curves is $\epsilon_r \sim 7$, which suggest that chemical reduction of the Al₂O₃ to Al_xO_y when the gate oxide makes physical contact with the top aluminum electrode occurs. The maximum capacitance at each frequency in the full range is different between one structure and another, as expected. The former is due to the difference in thickness of the aluminum oxide (C_g higher for Al₂O₃=10nm). This difference in thickness also influences the behavior of the capacitance C_g at low frequencies but most importantly, it also produce whether a higher degree of electrical instabilities or more uniform I-V characteristics as previously noticed. Therefore, not only the physical thickness of the gate oxide but also, the interfacial roughness of the Metal/Al₂O₃ interfaces must be taken into account in order to obtain reproducible and long lasting resistive switching properties for these memory devices.

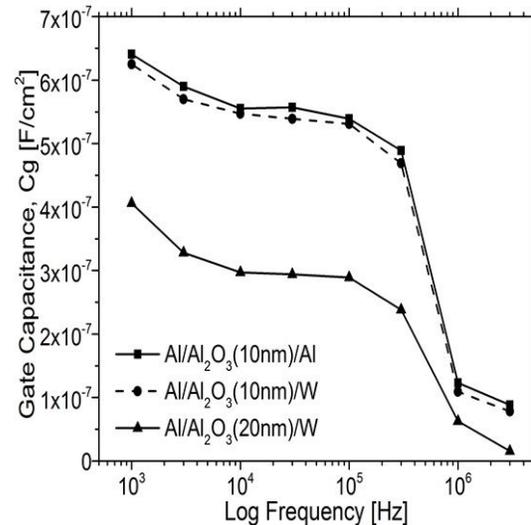


Figure 8. Dependence of gate capacitance C_g on frequency for Al/Al₂O₃/Al and Al/Al₂O₃/W systems.

Conclusions

Emergent memory devices which can be vertically integrated into a CMOS-based BEOL processing were fabricated using low thermal conditions and their electrical characteristics were obtained. Vertical integration of memory blocks would increase the integration density of advanced integrated circuits by one order of magnitude while getting close to a true 3-D type integrated circuit manufacturing. From these MIM devices, the memristor effect was observed and more than 4-6 orders of magnitude for the I_{OFF}/I_{ON} ratios have been obtained after cyclic I-V measurements for all structures. These broad conductivity/resistivity windows are important for long term trapping of carriers within the oxide and therefore, creation/dissolution of conductive filaments which then, will produce the switching between the HRS and LRS. Sharp differences in the conduction mechanisms (before breakdown) were also observed when using whether a highly reactive or an inert metal material as the bottom electrode. Along with the conduction mechanisms, the current compliance as well as the surface roughness of the bottom electrode plays an important role for reliable operation of these memory devices by obtaining reproducible V_{SET} and V_{RESET} conditions for cyclic voltage sweeps. Finally, an average dielectric constant of $\epsilon_r \sim 7$ was extracted from C-V measurements and which suggest a chemical reduction of Al₂O₃ to Al_xO_y when the gate oxide makes physical contact with the top and/or bottom aluminum electrode.

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